Claims

1. Method to perform a cycle synchronization between interconnected sub-networks, **characterized in that**

- a reference node connected to one of the sub-networks transmits a respective cycle time information to cycle masters of all other sub-networks at recurring time instants, and
- the cycle masters of all other sub-networks adjust their cycle time accordingly.

2. Method according to claim 1, **characterized in that** an adjustment of the cycle time within a cycle master is performed by the following steps:

- determining a first time interval (Δt_1, $\Delta t_1'$) in-between two receptions of cycle time information from the reference node with an own clock,
- determining a second time interval (Δt_2, $\Delta t_2'$) in-between two corresponding transmissions of cycle time information from the reference node on basis of the received cycle time information,
- comparing the first time interval (Δt_1, $\Delta t_1'$) and the second time interval (Δt_2, $\Delta t_2'$), and
- adjusting the own cycle length according to the comparison result.

3. Method according to claim 2, **characterized in that** the comparison of the first time interval (Δt_1, $\Delta t_1'$) and the second time interval (Δt_2, $\Delta t_2'$) considers a preceding adjustment of the own cycle length.

4. Method according to claim 2 or 3, **characterized in that** the adjustment of the own cycle length within a cycle master is performed in a step-wise manner.

5. Method according to claim 2, 3 or 4, **characterized in that** the adjustment of the own cycle length within a cycle master is performed by adjusting a local number of clocks within one cycle.

6. Method according to claim 5, **characterized in that** the adjustment of the own cycle length within a cycle master is performed by setting the local number of clocks

- equal to an ideal number of clocks of one cycle in case the first time

interval (Δt_1, $\Delta t_1'$) and the second time interval (Δt_2, $\Delta t_2'$) are identical,

- smaller than an ideal number of clocks of one cycle in case the first time interval (Δt_1, $\Delta t_1'$) is smaller than the second time interval (Δt_2, $\Delta t_2'$), and
- larger than an ideal number of clocks in case the first time interval (Δt_1, $\Delta t_1'$) is larger than the second time interval (Δt_2, $\Delta t_2'$).

7. Method according to claim 6, **characterized in that** a step-width to adjust the own cycle timer within a cycle master is set according to the difference of the first time interval (Δt_1, $\Delta t_1'$) and the second time interval (Δt_2, $\Delta t_2'$).

8. Method according to anyone of the preceding claims, **characterized in that** the cycle time information transmitted by the reference node is a content of its cycle time register.

9. Method according to claim 8, **characterized in that** the adjustment of the own cycle time within a cycle master is performed by adjusting the average difference between a time interval of two transmissions of cycle time information of the reference node which is determined by subtracting two succeeding received contents of the cycle time register of the reference node and a time interval of two samplings of the own cycle timer which is determined by subtracting two succeeding sampled contents of the own cycle time register plus a corrective difference to be zero.

10. Method according to claim 9, **characterized in that** the corrective difference corresponds to the preceding adjustment.

11. Method according to anyone of the preceding claims, **characterized in that** the recurring time instants are determined according to a regular time interval with a small variation.

12. Cycle synchronizator, **characterized by**

- a clock offset estimation means (1) to determine a timing error of an own cycle timer (3), and
- a cycle adjustment loop (2) receiving the timing error determined by said clock offset estimation means (1) to adjust the own cycle timer (3) to reduce its timing error.

13. Cycle synchronizator accordingto claim 12, **characterized by** a de-jitter filter (4) arranged in-between the clock offset estimation means (1) and the cycle adjustment loop (2) to filter said determined timing error.